## REMARKS

In the present application, claims 1, 3-9, 11-17 and 19-24 are pending. Claims 1, 3-9, 11-17 and 19-24 are rejected. Claims 23-24 have been canceled. As a result of this response, claims 1, 3-9, and 11-17, and 19-22 are believed to be in condition for allowance.

**Claim Rejections - 35 USC § 112**

The Examiner rejected claims 23-24 for failing to comply with the written description requirement. Specifically, the Examiner noted that the claims are directed to wireless communication devices while asserting that the specification does not disclose a wireless communication device. Claims 23-24 are canceled herein. As a result, the rejection of claims 23-24 is rendered moot.

**Claim Rejections – 35 USC § 103**

The Examiner rejected claims 1-3, 5-9, 11, 13-17 and 21-24 as being unpatentable over Earnest ('338) in view of what is well known in the art, as evidenced by Sato ('149), and in further view of Veenstra ('946).

While taking no position on the propriety of the Examiner's combination of Earnest, Sato, and Veenstra, each of the cited prior art references fail to teach a singular element recited, in various forms, in each of the pending independent claims. As such, the combination of the cited prior art likewise fails to teach or suggest the above noted claimed element.

With respect to claim 1, the Examiner asserts that a combination of the teachings of Earnest and Veenstra, such a combination being neither suggested nor recommended by the Applicants, recites the elements of claim 1. Specifically, the Examiner asserts that "Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode (RAM mode) and in FIFO mode

(Column 7, Lines 27-35) using same set of registers (column 9, Lines 20-32). Therefore, it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space."

Applicants respectfully disagree with the Examiner's characterization of the teachings of Veenstra vis-à-vis claim 1.

Claim 1 recites (in relevant part):

> an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory wherein in a first case said control unit operates individual ones of channel buffers in a block access mode of operation **using a set of channel registers and in a second case said control unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers.** (emphasis added)

Note that the claim recites "a set of channel registers" and not a channel register. It is clearly recited that a set of registers is used to control individual channel buffers in a block access mode, and that the same set of registers is used to control individual channel buffers in a FIFO access mode. In contrast, Veenstra makes clear that only a single register is employed in common when operating between FIFO and RAM mode. Specifically, at the Examiner's citation at col. 9, lines 19-27, it is stated "Additional logic is added to input data register 840 (shown in FIG. 8) to create **an** enhanced input data register 900 as shown in FIG. 9. The additional logic allows enhanced input data register 900 to operate in two separate modes. In RAM mode, it operates as a data register that latches whatever data is presented at the input. In the FIFO mode, enhanced data register 900 operates as a counter, incrementing its value by

one for each clock pulse when the increment (INC) line is asserted." (emphasis added). Note that one, and only one, register is utilized to operate in two separate modes.

As if to drive home the significance of the difference between the single register of Veenstra and the recited registers of claim 1, the Examiner specifically cites column 7, lines 24-34. There is recited at this citation "If a comparison of read address counter 512 and write address counter 514 shows the difference to be less than a defined value, then the FIFO is nearly full. **The defined value may be programmable** so that the application software is able to vary how full the FIFO is when it is warned of a nearly full condition by the hardware. A person of skill in the art can readily conceive of many alternative ways of accomplishing the same result. For example, **a separate counter may be used** that keeps track of the number of data values in the FIFO and the status may be derived in the separate counter." (emphasis added).

Note that, when specifically addressing the issue of storing threshold information when operating in a FIFO mode, Veenstra offers no hint of using one of a set of registers used in both FIFO and block access mode to store such information. In fact, as noted above, the existence of only one such register as taught by Veenstra renders such an option impossible. Once again, claim 1 specifically recites "wherein in a first case said control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and in a second case said control unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers."

Applicants agree with the Examiner's assertion that Earnest fails to disclose this element of claim 1. It is further clear that Veenstra fails to teach, or otherwise suggests, using the same set of registers when operating in both a FIFO and block access mode. Therefore, the combination of Veenstra and Earnest, such a combination not suggested by the Applicants, likewise fails to teach this element of claim 1. As a result, Applicants respectfully traverse the Examiner's grounds for rejection. Claim 1 is therefore in condition for allowance. As claims 3-8 depend upon claim 1, claims 3-8 are likewise in condition for allowance.

Claim 9 recites, in part, "using said set of channel registers in a first case to operate individual ones of channel buffers in a block access mode and in a second case using said same set of channel registers to operate said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation". For the reasons discussed above, claim 9 is in condition for allowance. As claims 11-14 depend upon claim 9, claims 11-14 are likewise in condition for allowance.

Claim 15 recites, in part, "where said control unit is programmable in a first case for operating individual ones of said buffers in a block access mode of operation and operating in a second case said individual ones of said buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers". For the reasons discussed above, claim 15 is in condition for allowance. As claim 16 depends upon claim 15, claim 16 is likewise in condition for allowance.

Claim 17 recites, in part:

> said control unit being responsive to operating in a Block Mode to provide two independent buffers Buffer0 and Buffer1, where BaseReg0 stores the starting address of Buffer0, SizeReg0 specifies the size of Buffer0, BaseReg1 stores the starting address of Buffer1, and SizeReg1 specifies the size of Buffer1 size, said control unit being further responsive to operating in a FIFO Mode to provide one buffer, where BaseReg0 stores the start address of the single buffer, SizeReg0 specifies the size of the single buffer, BaseReg1 functions as a Low Threshold Register, and said register SizeReg1 functions as a High Threshold Register.

For the reasons discussed above, claim 17 is in condition for allowance. As claim 22 depends upon claim 17, claim 22 is likewise in condition for allowance.

Claim 19 recites, in part, "wherein a single set of channel registers controls the operation in said block mode and in said FIFO mode". For the reasons discussed above,

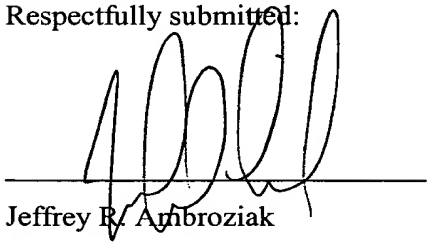
claim 19 is in condition for allowance. As claim 20 depends upon claim 19, claim 20 is likewise in condition for allowance.

Claim 21 recites, in part, "wherein in a first case said controlling means operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and in a second case said controlling means unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers." For the reasons discussed above, claim 21 is in condition for allowance.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

Respectfully submitted:



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